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PICMOS

Photonic Interconnect Layer on CMOS by wafer-scale integration

STReP - Specific Targeted Research Project

IST – Information Society Technologies

D1.2. Definition and quantification of specifications for different subcomponents

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1. Introduction

The aim of deliverable D1.2 is to describe the work undertaken in WP1 to define and quantify the specifications for the various subcomponents in the PICMOS integrated optical link. This required the development of models and tools to design and optimise optical and electrical interconnect in a range of technologies and under a range of specification conditions, in order to evaluate the properties of the technologies developed, to compare them to the performance of current and future electrical interconnect alternatives in terms of important performance metrics (mainly area, data rate and power), and finally to determine the specifications for which the proposed technologies would outperform traditional interconnect. Optical-electrical interconnection comparison is not new: several authors have already published comparative studies between optical and electrical on-chip interconnect technologies [COL2000] [FRI2001] [KOB2004]. Most of those consider expected technological evolutions to provide a roadmap of interconnect performance. This is done either by using analytical models, or by a simulation-based approach. Analytical models are usually based on ITRS[*] [ITR2005] future CMOS technology parameters or other expected future CMOS technology parameters and rough estimates of optical interconnect performance. Simulation models are either self-constructed, based on ITRS parameters [COL2000], or using publicly available Predictive Technology Models (BPT - now for gate lengths ranging down to 32nm [CAO2000]).

In this work, as it was intended to be able to determine device-level specifications, it was necessary to generate accurate optical link performance estimates that can be traced back to individual component parameters. Part of the optical link consists of analog CMOS circuitry. The design thereof can be done based on analytical models, but it is very sensitive to MOSFET parasitics so it is crucial that these parameters are available. However, the data presented in the ITRS is intended for digital design applications. This implies that estimates on transistor parasitics are very rough or in some cases not even available. Hence, for an accurate evaluation, it is best to use technologies for which simulation models are available.

This still leaves the option to use analytical models for the electrical interconnect evaluation. Indeed, analytical models are acceptable for deriving scaling trends and they are still quite accurate for estimating link delay, static power or capacitive switching power. However, our analyses have shown that model based estimates of more sensitive link properties such as short-circuit power dissipation and cross-talk induced jitter only very poorly match simulation-based results.

For the reasons mentioned above and because we wanted to come up with link performance results that were as comparable as possible, we have decided to use a simulation based approach for both technologies. We have used predictive technology models with gate lengths from 130nm down to 32nm, as well as simulation models for industrial technologies with 130nm and 100nm gate lengths (for comparison). In contrast

[*] International Technology Roadmap for Semiconductors (http://public.itrs.net)

to the model based approaches, our choice implies that we cannot stretch our analysis beyond 32nm gate lengths. However, according to the ITRS, a 32nm gate length technology (which is the smallest available transistor model on the BPT website) would be taken into production for high-end applications in 2008, and this is only the beginning of its lifetime. Therefore we claim that our analysis does stretch sufficienly far into the future. Also, by observing trends in performance metric evolution over technology node it is possible to extrapolate the analysis to future technology nodes with a good degree of certainty.

The models and software developed were therefore made to be sufficiently generic in order to enable a) the exploration of performance capabilities of optical links with existing technological constraints; and b) the impact of improvements in device performance on interface circuit sizing and overall link performance. This replaces the original objective of "generating specifications to be taken into account in the component and integration oriented workpackages" by giving a richer set of data. This allows tradeoffs to be understood, as well as their relevance in the context of overall link performance metrics.

This document begins in section 2 by describing the context of the analysis in terms of the considered application (on-chip long-haul parallel interconnect) defined in D1.1 by CNRS-LEOM and IMEC, and the basic topologies of the electrical and optical interconnect links. The generation of optical link parameters based on link specifications is based on analog synthesis techniques, and section 3 describes CNRS-LEOM's contribution to develop an open hierarchical multi-domain synthesis platform with simple specification models. This tool allows the creation of hierarchical design/optimisation methods for each component block. Through their association, it is possible to create design scenarios to create a global concurrent synthesis flow.

To enable simulation, a number of behavioural models were developed by IMEC (sources) and CNRS-LEOM (waveguides and detectors) enabling complete photonic link simulation at CNRS-LEOM. This work is described in section 4. The optical link synthesis methods are described in section 5 and exploit the simulation work to generate performance metric data for considered technologies and optical link lengths. The electrical interconnect synthesis toolset is described in section 6, and results are compared in section 7. Through identification of the impact of individual device parameter variations on particular performance metrics, an exploration of these variations is shown in section 8.