FP6-2002-IST-1-002131

PICMOS

Photonic Interconnect Layer on CMOS by wafer-scale integration

STReP - Specific Targeted Research Project

IST – Information Society Technologies

D2.3 - Report on die fabrication and preliminary bonding results

Due date of deliverable: M18 – June 30, 2005

Start date of project: January 1, 2004 Duration: 36 Months
Lead Contractor : TRACIT Technologies Revision: Final
Contribution Partners: CEA-LETI, IMEC, NCSR-D

Dissemination Level: *Confidential, only for members of the consortium (including Commission Services)*

ABSTRACT

As previously described in D2.1 and D2.2 reports, 3 bonding techniques are developed in PICMOS project to assemble the different parts of materials and components, with the final aim to integrate photonic components on CMOS devices. The work package 2, in charge of bonding developments gathers four partners specialized into different techniques:

- ☐ CEA-LETI / LTFC : direct molecular bonding (essentially focusing onto die-to-wafer bonding)
- ☐ IMEC : BCB bonding
- ☐ NCSR-Democritos : metallic bonding
- ☐ TRACIT : direct molecular bonding (essentially focusing on structured wafer-to-wafer bonding) + WP2 leader (industrial evaluation of the different bonding technologies)

The deliverable deals with die fabrication and bonding onto wafer.

Two different bonding steps are involved in PICMOS process.
First bonding step concerns the bonding of opto-electronic dies (with epitaxial layers dedicated to source or detector components) onto waveguide wafer: as there is no need of electrical contact between both sides, metallic bonding is not involved into this step; BCB or molecular bonding may answer to the specifications of this first assembling. The results presented by CEA-LETI and IMEC will treat about this first step.
After elaboration of photonic components, another bonding step is needed to join the photonic layer onto the CMOS wafer. The 3 bonding techniques can be used at this step. Metallic bonding is particularly interesting here because it may allow a direct electrical connexion between pads on photonic components and CMOS. As drawn on the figure 1, this step should involve a wafer to wafer bonding. In the particular configuration of the project, all the processing of the photonic layer will be made on samples whose size will be around 2*2cm², instead of 200mm wafers. Thus, developments have been done to bond samples (“large dies”) onto wafers, at this second bonding stage; that’s why the related results will be discussed in this deliverable which deals with “die fabrication and die to wafer bonding”. The results presented by NCSR-D on metallic bonding will focus on this topic.

The presented results are very interesting and encouraging.
Concerning the first bonding step, molecular bonding appears compatible with the assembling of optoelectronic dies onto wafers. Some investigations remain to be done on different epitaxial layers (dies). Demonstration of the possibility to bond dies onto wafer via BCB has also been made. Additional work remains concerning bonding reproducibility and compatibility with subsequent thinning down processes.
Concerning the second bonding step (photonic layer onto CMOS wafer), a variety of experiments for metallic bonding using patterned wafers and dies have been successfully completed and electrical connectivity parameters have been estimated. The next step is the further development of the die-to-wafer alignment procedure.
No technical issue is encountered at this stage of the project.