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PICMOS

Photonic Interconnect Layer on CMOS by wafer-scale integration

STReP - Specific Targeted Research Project

IST – Information Society Technologies

D2.4 - Report on the developed techniques for die to wafer bonding

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Lead Contractor : TRACIT Technologies
Contribution Partners: CEA-LETI, IMEC, NCSR-D

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Dissemination Level: *Confidential, only for members of the consortium (including Commission Services)*

ABSTRACT

The global process flow for PICMOS demonstrator was defined at the end of the second year period (Milestone 2.1). Molecular bonding was chosen for the first bonding step of optoelectronic dies onto waveguide. For the second bonding step used to assemble photonic component onto CMOS wafer, metallic bonding was chosen as it allows direct electrical connection via bonding pads. However, this deliverable deals with the 3 bonding techniques developed within WP2 (including BCB bonding) as the final technological choice emerged at the end of the second year period.

Molecular bonding developments (performed by CEA for die bonding aspects and by TRACIT Technologies for full wafer bonding aspects) have reached requirements specified within PICMOS project. Bonding quality and bonding strength were checked with InP wafers having in-coming defined characteristics (low roughness and low bow). Bonding tests were made on dies with dimensions going from $2mm^2$ to $1cm^2$. An alignment accuracy inferior to 50µm could be achieved using pick and place equipments. A significant number of bonded dies showed a good reproducibility of this technology. Concerning dimensional requirements on thickness and uniformity of intermediate oxide layer between III-V die and waveguide (specifications determined by components workpackages), equipments qualifications and process developments were performed to reach targeted values. Regarding to post-process compatibility, few tests were performed on III-V bonded layer or dies to verify the integrity of the transferred film: all indicators (optical control or photoluminescence cartography…) confirmed the good quality of the thin layer after substrate removal. Very few tests have been done with the full processing of photonic components: this work will be mainly performed during the third year as WP3, WP4 and WP6 components will be completed.

BCB bonding was developed by IMEC as an alternative to the direct molecular bonding approach. Major part of results reached PICMOS specifications. To address the different components requirements, two processes were developed: one based on thick BCB layer (3µm) and another one using thin BCB layer around 200nm-300nm. Technical issue arose with this last process regarding to reproducibility; as BCB layers were very thin, particle contamination appears as a critical point to perform good bonding quality. This problem mainly influenced the final choice of molecular bonding for the first bonding step of PICMOS global flow. The fact that BCB bonding can not be applied to 200mm wafer at the moment argue also in the way not to use it in the fabrication of the final demonstrator of the project.
Die size varied from a few mm^2 to $1cm^2$. Positioning of dies on the substrate with accuracy better than 50µm was achieved. The transfer of an SOI optical waveguide layer using BCB was demonstrated, with very little degradation in optical characteristics.

Metallic bonding was developed by NCSR-Demokritos in view of the second bonding step of PICMOS global flow. Objective was to achieve a direct electrical connection between photonic part and CMOS via metallic bonding pads. Properties of the alloy have been defined: composition based on 80Au-20Sn was fixed, 9 successive layers were deposited to form final bonding pads on each wafer to be assembled, with an intermediate layer of Gd between the alloy and the wafers surface. The alloy patterning process was repeatable and lead to well-defined features. Bonding feasibility was proved on various surfaces (Si, SiO_2, BCB). Passive alignment, aided by infrared imaging, between concave and convex alloy formations present on assembled surfaces lead to good preliminary results. And finally, from an electrical point of view, connectivity between top and bottom wafers was checked. Specifications are thus globally fulfilled for this bonding stage.