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PICMOS

Photonic Interconnect Layer on CMOS by wafer-scale integration

STReP - Specific Targeted Research Project

IST – Information Society Technologies

D6.1 - DESIGN OF THE PHOTONIC LINK

Due date of deliverable: M24 – Actual: M25

Start date of project: January 1, 2004 Duration: 36 Months
Lead Contractor : CEA Revision: Final
Contribution Partners: All partners

Dissemination Level: *Confidential, only for members of the consortium*

I Public Abstract

Workpackage 6 integrates the major achievements of the PICMOS-project. It builds further on the results obtained in the other workpackages and combines them with the goal of conclusively demonstrating the feasibility of adding a photonic interconnect layer on top of future generation electronic ICs. Therefore, the demonstrator is composed of

- An optoelectronic die containing optical links, consisting of µsources and detectors, connected through a direct passive optical waveguide or through a 1→8 passive waveguide distribution network.
- An optoelectronic assembly consisting of optoelectronic dies metallically bonded on a CMOS wafer acting as a base for electric tests.

This demonstrator design is the fruit of extensive discussions between partners based on the results already obtained and on the need of reducing the risks of a new complex fabrication. In most of the workpackages, several alternatives were proposed and at M21 these choices has been made to start the design of the demonstrator.

- As the beginning of the project, two basically different business models were proposed: a parallel wafer-to-wafer integration scheme where the photonic interconnect layer and the CMOS wafers are bonded together only in the final stage, and a serial above-IC integration scheme where the photonic interconnect layer is fabricated directly on top of a CMOS wafers. The choice between these two options relied on the waveguide choice. As excellent results were obtained in WP5 for both SiNx and Si technologies, the choice for Si waveguide has been made considering the easier coupling to the µdisk or DBR source of WP3.
- So the parallel option was selected, but due to the fact that InP technology could not be processed on a 200m format and that big dies of 2cm2 were required for that, a four step fabrication process was chosen with metallic bonding of these big optoelectronic dies on scrap CMOS wafers with upper metallizations.
- Molecular bonding was chosen from WP2 in view of the excellent results of the die-to-wafer bonding technique developed in WP2 using molecular bonding, which showed for example good reproducibility on the separation between waveguide and source.
- For the sources, the ultracompact type (either DBR or µdisk) was selected because both their integration with silicon waveguides and electrical contacting was demonstrated (albeit in separate demonstrators).
- The selected PD structure is built as an InGaAs absorption layer sandwiched between a pdoped InGaAs layer on top and an n-doped InP layer underneath. An InP membrane input waveguide on top of the bonding layer is used to couple the optical signal from the photonic waveguide layer to the PD structure, which is stacked on top of the input waveguide itself

A detailed processing flow was defined and divided in four steps: Fabrication of the silicon waveguide wafers (200mm), die-to-wafer bonding and ebeam lithography (200mm), fabrication of photodetectors and µlasers (2cm2) and bonding of the photonic dies to scrap CMOS wafers (200mm & 2 cm2)

From this process flow, the design of the photonic die was started with all partners. The optical chip is based on a 7x9mm^2 SOI die containing the waveguide circuitry. Both sources and detectors are grouped in blocks of 8 devices. Fifteen source blocks are dedicated for microdisk lasers and 15 for DBR-microlasers. Detector parameters change mainly within the 33 detector blocks. Six source and six detector blocks are connected to RF-contact pads, to allow high-speed modulation measurements. After fabrication, the photonic die will be integrated with metal pads on scrap CMOS wafers via metallic bonding. The choice has been made to process two levels of Cu metallization on scrap CMOS wafers and to define alloy layers both on the pads of the photonic die and the scrap CMOS wafer. CMOS and optoelectronic die topology are assessed in order to define the appropriate bonding process specifications.