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PICMOS

Photonic Interconnect Layer on CMOS by wafer-scale integration

STReP - Specific Targeted Research Project

IST – Information Society Technologies

D2.1 - Report on the different techniques evaluated to bond InP wafers onto silicon wafers

Public Part of Confidential Deliverable

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PICMOS PROJECT – Work Package 2

D21: Report on the different techniques evaluated to bond InP wafers onto silicon wafers

PUBLIC ABSTRACT

The objective of PICMOS project is to demonstrate the feasibility of adding a photonic interconnect layer on top of silicon CMOS circuitry, in a way which is compatible with the processing of advanced electronic integraded circuits, both in terms of fabrication and in terms of cost. This radically different interconnect approach is expected to give solutions concerning the global interconnect level, for future generation electronic circuits.
One integration strategy investigated in this project consists into "wafer-to-wafer bonding approach". This approach includes the fabrication of the photonic layer (bonding of opto-electronic components onto waveguide wafer) and its bonding onto the CMOS wafer (via bonding and substrate back removal). The wafer and die bonding processes are developed in the Work Package 2, which gathers four partners, specialized into different bonding technologies:

- ☒ CEA-LETI / LTFC : direct molecular bonding (essentially focusing onto die-to-wafer bonding)
- ☒ IMEC : BCB bonding
- ☒ NCSR-D : metallic bonding
- ☒ TRACIT : direct molecular bonding (essentially focusing on structured wafer-to-wafer bonding) + WP2 leader (industrial evaluation of the different bonding technologies)

In the classical approach, a first bonding step is necessary to join III-V components to the waveguide substrate, to form the photonic wafer. Different opto-electronic structures (III-V) will be studied and developed in the project: namely, micro-sources and detectors. Depending on the type of component, the requirements on the bonding step can be different: that's the reason why various bonding techniques are evaluated in parallel. In particular, direct wafer bonding and BCB bonding will be the main techniques evaluated for the photonic layer fabrication.
A second bonding step is required for the assembly of the photonic wafer onto the CMOS wafer; at this stage, molecular bonding, BCB and metallic bonding will be studied.
The objective of this deliverable was to evaluate the different bonding techniques, for full wafers or large dies.
An important effort has been done from the beginning of the project to define technical specifications for the bonding characteristics, which can serve as a guideline for all the WP2 partners, to develop and optimize their technologies. These specifications were determined in collaboration with all the partners of the PICMOS project and are specified within this deliverable.

After a short overview of general characteristics of bonding techniques developed in WP2, including bibliography on know-how, advantages and drawbacks regarding to the project, each partner has described the results obtained on full wafer bonding or large dies of InP substrates onto Si substrates.
Concerning direct bonding technology, developed by CEA/LETI/LTFC, a process has been developed for full epitaxial III-V wafer bonding onto silicon via a SiO_2 layer. Various types of SiO_2 layer were studied as bonding layers (in terms of bonding interface quality and strength) to enlarge process possibilities. The first demonstration of direct bonding of a die (with dimensions within project specifications) on a wafer was performed.
IMEC worked on the use of a spin-on intermediate layer for bonding (BCB, SOG, polyimide…): after several studies and developments, they essentially focused on BCB bonding because of most encouraging results. All experiments were carried out using III-V wafer pieces (~1 cm^2). Stress and general quality of the bonded membrane where judged by fabricating simple optoelectronic devices in the film and comparing them with standard devices.
Metallic bonding was investigated by NCSR-Democritos: developments were performed on various Au/Sn alloy compositions (evolution of surface roughness as a function of composition). Precise alloy composition has been achieved, leading to flat Si and InP dies bonding onto flat Si wafers, with solder joints thicknesses ranging from 0.1 to several µm.

These first results obtained by the different partners, on full wafer or large die bonding are quite encouraging. After 8 month, we can say that we have three different technologies which are generic and which can be used for the demonstrator assembling. In a table, the advantages and drawbacks of each technology were summarized and its possible application for the different bonding steps needed in the context of the project were described. The choice for the final bonding technology to be used for the demonstrator is still open, and will be dependent both on the outcome of the following work in WP2 (bonding of small dies and bonding of structured wafers) and on the final definition of the global demonstrator integration process.

In the next months, each partner will continue to work on its technology focusing its study on the bonding of small dies onto wafer, on the bonding of patterning wafers and on the reliability on the processes.