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PICMOS

Photonic Interconnect Layer on CMOS by wafer-scale integration

STReP - Specific Targeted Research Project

IST – Information Society Technologies

D2.2 - Report on bonding structured wafers

Public Abstract

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Dissemination Level: *Confidential, only for members of the consortium (including Commission Services) – Abstract can be freely distributed*

ABSTRACT

The objective of the PICMOS project is to demonstrate the feasibility of adding a photonic interconnect layer on top of silicon CMOS circuitry, in a way which is compatible with the processing of advanced electronic integrated circuits, both in terms of fabrication and in terms of cost. This radically different interconnect approach is expected to give solutions concerning the global interconnect level, for future generation electronic circuits.
The integration strategy investigated in this project is based on a "wafer-to-wafer bonding approach". This approach includes the fabrication of the photonic layer (bonding of opto-electronic components onto waveguide wafer) and its bonding onto the CMOS wafer (via bonding and substrate removal). The wafer and die bonding processes are developed in the Work Package 2, which gathers four partners, specialized into different bonding technologies:

- ☒ *CEA-LETI / LTFC : direct molecular bonding (essentially focusing onto die-to-wafer bonding)*
- ☒ *IMEC : BCB bonding*
- ☒ *NCSR-D : metallic bonding*
- ☒ *TRACIT : direct molecular bonding (essentially focusing on structured wafer-to-wafer bonding) + WP2 leader (industrial evaluation of the different bonding technologies)*

In the previous D2.1 report, treating the different techniques evaluated to bond InP wafers onto Silicon wafers, the different partners have described the results obtained on bonding of large dies or substrates of InP onto Silicon substrates. These results essentially concerned the elaboration of the photonic layer. However, at this stage, the wafer on which dies were bonded was flat, without topology.

In this second report (D2.2), we will focus on another bonding step involved into the PICMOS integration approach, namely the assembly of patterned wafers or of dies on patterned wafers. The wafers to be bonded are exhibiting surface topology, so specific preparation is needed. Furthermore, alignment may be required between both patterns. This step is needed for the fabrication of the photonic wafer (dies onto patterned waveguide wafer) and also for the bonding of the completed photonic wafer onto the CMOS wafer (in the parallel integration approach).

TRACIT demonstrated the possibility to assemble patterned wafers via a SiO2 bonding layer thanks to direct molecular bonding. Furthermore, the bonding strength obtained after low temperatures treatments, exhibited total compatibility with next thinning down steps (by mechanical and chemical ways). Bonding ability regarding to different surface topologies (from few 100th nm to few µm) was evaluated. Direct wafer bonding offers the opportunity to join wafers having a large range of patterns and topology.
Further process qualifications have to be carried out on the "copper dedicated equipments" to improve the bonding and transfer quality, as CMOS wafers to be assembled to photonic layers will be elaborated with copper interconnections technology.

IMEC demonstrated the possibility to assemble patterned wafers via a spin-on bonding agent (BCB). For thick bonding layers (>2µm), surface topology over 1µm can be tolerated. In addition, the existing bonding technology was extended towards thinner bonding layers. Currently, the possibility for bonding small dies is investigated.