Metallic bonding of optoelectronic dies to silicon wafers

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Abstract In future generation electronic circuits the severe bottleneck which is expected on the level of interconnections seems to has only one possible solution: that of using optical interconnection layers instead of the electrical ones. Our research focuses on the development of a die-to-wafer metallic bonding technique for the integration of a photonic wiring circuit on top of the CMOS wafer. Metal plating of the contact surfaces of both the optoelectronic devices and CMOS wafer pads using appropriate alloys are examined. After experiments with different metal alloys we decided to proceed with Au/Sn deposition on both CMOS and III-V photonics. Precise alloy composition has been achieved with multilayers and flat Si and InP dies have been successfully bonded on flat Si wafers using either hard Au-20Sn or soft Au-39Sn and Au-71Sn with solder joints thickness ranging from 0.1 to several μm. Experiments aiming to the study of alloys incorporating rare earths and their influence to the properties of the metallic bonding have been performed. Initial encouraging results are reported.

1.Introduction

High-density hybrid integration of III-V compound optoelectronics (OE) with Complementary Metal Oxide Semiconductor (CMOS) Integrated Circuits (ICs) is emerging as a technology able to provide the features and performance required by the next generation of high functionality information processing subsystems. Though the performance potential of III-V OE is widely recognized, high density co-integration with CMOS and low-cost manufacturability remain the key issues, which will ultimately determine the potential of this technology for market penetration [1]. A novel approach with the above mentioned characteristics is the integration of a photonic layer on top of CMOS electronics [2]. The photonic layer comprises active III-V devices bonded on an appropriately patterned waveguide substrate and is fabricated in parallel with CMOS ICs.

In this paper a metallic bonding technique is proposed which can be used for the integration of the photonic layer on the CMOS wafer. The main feature of the metallic bonding is that metal plating of the contact surfaces of both the optoelectronic devices and CMOS wafer pads using an appropriate alloy provides the required means for bonding the two wafers due to solid state intermetallic fusion. Moreover, if necessary, electrical interconnections can be formed at the same bonding step and good thermal conductivity is achieved. Initially, in section 2 the comparison and selection of alternative metal alloys is discussed. The analysis of the metallic bonding procedure is presented in section 3 and experimental results are given. Finally, in section 4 the conclusions are drawn.

2.Metal alloys

An overview on the various metal alloys characteristics and on their compatibility with the processing of advanced electronic integrated circuits turned out that desirable properties of the metal

alloys to be used for metallic bonding are the following: 1) alloys should be Pb free and the process should be fluxless (environmental friendly), 2) the bonding should be eutectic (or have small plastic range), 3) alloys should have low melting point to insure the safety of CMOS and optoelectronic devices already fabricated, 4) bonding scheme should insure slow growth of intermetallic compound (IMC) at the solder joints for reliability. An additional parameter, which is considered, is the utilization of either soft solder (to relax the stress/strain by plastic deformation) or hard solder (for high yield strength resulting in elastic deformation).

From the multitude of Pb free alloys the Au -based systems have been selected to be examined due to better known characteristics. Popular Au based solders are the Au/Sn, Au/Ge and Au/Si alloys. For reasons of low thermal fatigue and high reliability, Au/Sn solder is commonly used. As a hard solder it remains in elastic deformation and the TEC mismatch becomes important only when bonding large chips [3]. The advantage of the Au/Sn alloy over other hard solders is its comparatively low melting point (T_m =280°C) allowing it to be used along with temperature sensitive materials. Eutectic Au-20Sn solder is more and more used for Flip Chip assembly especially of OE devices because no flux is necessary during soldering [4]. Moreover, from the ASM binary phase diagrams [5] of the Au/Sn alloy it is clear that Au-20Sn solder is advantageous due to his lower melting temperature.

In summary, after careful examination of a variety of the above-mentioned Au combinations we decided to closely investigate the Au/Sn alloy for the following reasons: 1) provides great joint strength to reduce thermal fatigue (absence of underfill), 2) offers superior resistance to corrosion, 3) is compatible with III-V metallizations and 4) has already been successfully used to bond flat Si and InP wafers [6] for VCSEL fabrication.

Moreover, the ability of rare-earth-containing lead-free solders to wet and bond to silica was investigated. Small additions of Lutetium (0.5–2 wt. %) added to eutectic Sn–Ag or Au–Sn solder render it directly solderable to a silicon oxide surface [7]. The rare-earth element migrates to the solder–silica interface for chemical reaction and an interfacial layer that contains a rare-earth oxide is created. Since it was found that additions of rare-earth materials did not significantly modify the solidification microstructure or the melting point the possible advantage of their use in the bonding procedure are examined. After examination of a variety of the rare earth elements available in the market we decided to investigate the Holmium (Ho) and Gadolinium (Gd). Unlike Lutetium (Lu) which is the hardest, densest and one of the rarest of the lanthanides group of elements, Ho and Gd have lower melting point and their lower cost and availability make them attractive for a collective process. Some physical properties of Ho and Gd that justify our choice are listed in table 1.

Table 1: Holmium and Gadolinium properties.

	Holmium	Gadolinium
General description	soft and malleable and it is slowly attacked by oxygen and water	stable in a dry atmosphere and has magnetic properties
Melting point (^oC)	1474	1313
Thermal expansion coefficient ($x10^{-6}/K$)	9.5 @ 0-400C	6.4 @ 0-100C

3.Experiments

In the proposed approach for the metallic bonding the CMOS wafer has to be patterned with photoresist. Then Ti(adhesion layer)-Ni or Pt (diffusion barrier)-Ti-Au metal layers are deposited, by e-beam evaporation, on the Al pads, which will host the III-Vs components. Pd based (Pd/Ge/Sn or Pd/Ge/In/Sn) metallization can be used on the III-V devices to form ohmic contacts (if required). Sintering is performed at 300^{o}C in N_2 atmosphere. Hence, Au from the CMOS pad and Sn from the III-V metallization form the metal joint. Additionally, Ge diffuses through Pd forming PdGe non-alloyed ohmic contact (if required).

Experiments were performed on plain Si wafers with the metallization scheme consisting of Au and Sn and with a Ti adhesion layer. Indeed, results demonstrated that Au (from the CMOS pad) and

Sn (from the III-V metallization) form AuSn alloy after reflow. However, often this procedure results in deficient metal intermixing and poor control of the AuSn alloy composition. Therefore next tries were performed with a multilayer Au/Sn deposition on both CMOS and III-V photonics for accurate alloy composition The sample preparation contains the following steps: cleaning with acetone, methanol, isopropyl alcohol, deionized water and ultrasonic agitation, deposition by e-beam of thin Ti adhesion layer, deposition by e-beam Au/Sn multilayers and reflow in a Biorad RC2400 alloying furnace under a 95%N_2 5%H_2 flow. Systematic experiments have been performed with three Au/Sn alloy compositions of interest (Au-20Sn, Au-39Sn and Au-71Sn as determined by EDX) and with various metal thicknesses (ranging from 0.1 μm to several microns). Metals are deposited with a Temescal type e-beam evaporator in a vacuum chamber at 10^{-7} Torr. Annealing temperatures were chosen according to Au/Sn ASM phase diagram. For submicron thickness solder the samples are sintered for 45 min under pressure. The following SEM micrographs (figure 1,2,3) depict the surface of the samples for the three alloy compositions and for a thickness of metallization of 0.25μm. The details for each deposition for the three alloy compositions are shown in table 2.

Table 2: Parameters for the deposition of Au/Sn multilayers.

composition	Au /Sn Thickness	No of repeats	Total thickness	Annealing temperature	RMS roughness (nm)
80% Au / 20% Sn	30nm Au /20nm Sn	5	250 nm	280 ^{0}C	8.73
61% Au / 39% Sn	15nm Au / 20nm Sn	7	245 nm	250 ^{0}C	12.77
29% Au / 71% Sn	5nm Au / 20nm Sn	10	250 nm	220 ^{0}C	48.93

Figures 1, 2 and 3 show that the surface roughness increases with Sn content. The same effect is observed with metallization thickness.

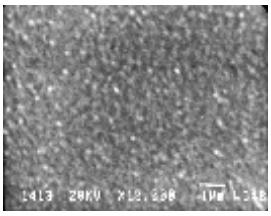

Figure 1: SEM photo of Au-20Sn surface.

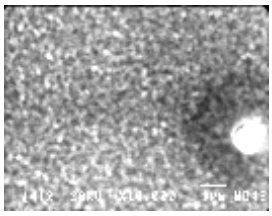

Figure 2: SEM photo of Au-39Sn surface.

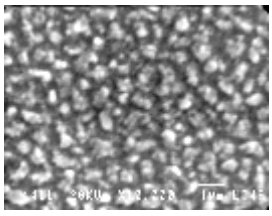

Figure 3: SEM photo of Au-71Sn surface.

Additional characterizations have been performed using AFM and the respective measurements are given in the last column of Table 2. Moreover, Nomarski optical microscopy characterization was performed. The resulting photos revealed that the best surface profile before and after the annealing step for the three alloys was achieved for the Au-20Sn metallic composition. Figure 4 presents the cross section of a flat Si die bonded on a flat silicon wafer using hard Au-20Sn alloy without the use of any adhesion layer. Finally, the crack opening method results showed very satisfactory bonding strength (>2J/m^2).

In a real OE system photonic dies and CMOS wafers are patterned, thus metallic pads should be fabricated on both of them to enable bonding. Initially the ability of the metal alloy to form well-controlled structures is investigated by fabricating square and circular pads of different dimensions. The SEM pictures of large (200μm) and small (70 μm) pads using the Au-20Sn alloy are shown in figures 5 and 6. The next step, which is currently under investigation, is the use of active and/or passive alignment techniques to make possible the bonding of samples with pads.

Incorporation of rare earths in the metallization schemes has been successfully demonstrated and promising results from Si to Si wafer bonding experiments have been obtained. It should be noted that the addition of (2-4 wt %) of Gadolinium and Holmium does not significantly modify the solidification microstructure or the melting point of the metal alloy. Therefore, high chemical reactivity of rare earths can be exploited in the metallic bonding procedure to increase the bonding energy.

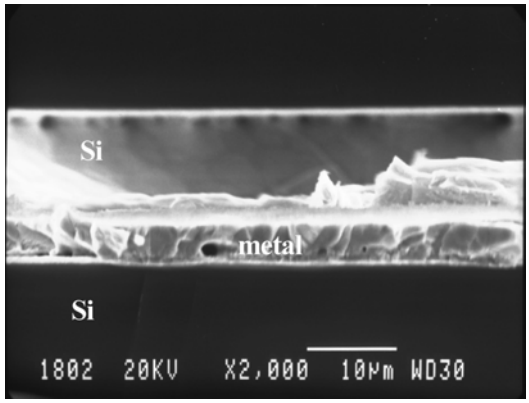

Figure 4: Cross section of Si to Si bonded dies.

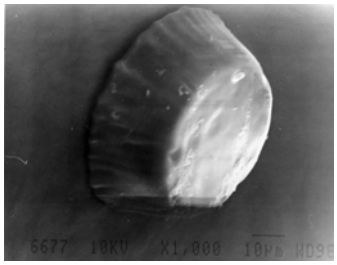

Figure 5 : 70 μm pad.

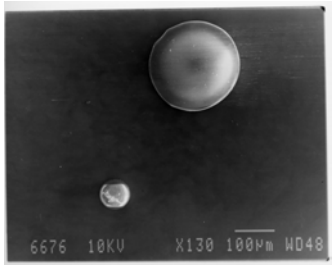

Figure 6 : 200 μm pad.

4.Conclusions

In summary, precise alloy composition has been achieved with multilayers and flat Si and InP dies have been successfully bonded on flat Si wafers using either hard Au-20Sn or soft Au-39Sn and Au-71Sn with solder joints thickness ranging from 0.1 to several μm. The eutectic Au-20Sn was adopted for corrosion resistance and mechanical strength without plastic deformation. Moreover the formation of small pads with the use of the proposed alloy proved to be quite successful. Finally, characteristics such as high bonding strength and absence of any additional adhesion layer when using additions of rare earths are strongly compiling to continue further research in that area.

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