Heterogeneous integration technique of optoelectronic dies to CMOS circuits via metallic bonding

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Abstract

The integration of complete optoelectronic dies, consisting of optical sources and detectors connected by waveguides for the employment of a photonic layer above CMOS integrated circuits has been proposed. Photonic dies are integrated to CMOS circuits through a novel metallic bonding technique that utilizes a thin multilayer structure of the Au-20Sn eutectic alloy along with a starting layer of a rare earth element (Gd). Its main advantage is the accomplishment of mechanical bonding and electrical connectivity of the heterogeneous devices in a single step. In this paper results on bonding quality and electrical characterization are presented

Introduction

The ability of the industry to exponentially decrease the minimum feature sizes used to fabricate integrated circuits (ICs), has already began to transfer the bottleneck of high speed performance from the active devices to the electrical interconnect [1]. Propagation delay due to wire resistance-capacitance (RC) poses serious performance degradation in the global or even the intermediate interconnect regime. On the other hand, as supply voltage is reduced, crosstalk has become an issue for all clock and signal wiring levels [2]. Traditional interconnect scaling will suffer in satisfying performance requirements. Defining and finding solutions beyond copper and low-k materials requires unconventional interconnect in the intrachip level, as well as alternative packaging in the interchip level.

A possible solution is the use of three-dimensional (3-D) optical interconnect technologies. Heterogeneous integration of III-V compound optoelectronics (OE) with complementary metal oxide semiconductor (CMOS) ICs in high-density parallel links can meet the performance challenges of future computational systems [3-5]. Optical interconnections achieve lower propagation delay, high switching bandwidth as well as minimal electromagnetic interference (EMI). OE-CMOS IC integration architectures include 3-D assembly of stacked dies through various technologies, such as the flip-chip, epitaxial lift-off (ELO), applique or fluidic self-assembly [6-7]. A number of successful integration attempts using the former technologies have been published [8-12]. The use of complete OE dies consisting of optical sources and detectors connected by waveguides for the employment of a photonic layer above CMOS ICs has been proposed [13]. In this paper, a metallic bonding methodology is introduced for bonding OE dies above CMOS circuitry. A multilayer structure of the Au-20Sn eutectic alloy over a thin film of Gd is proposed as bonding agent.

In Section I, the properties and structure of the alloy that is proposed as the bonding medium are analyzed. Pattern uniformity is addressed and spreading tests are described in Section II. Bonding experiments and quality tests are described in Section III and electrical connectivity measurements are presented in Section IV.

I. Alloy properties and structure

Environmental friendly processes restrict solders used in packaging to the Pb-free group. On the other hand, successful flip-chip assembly is favored by eutectic alloys. Since die attachment is realized by solder fusion, a low melting point is desirable for CMOS and OE devices thermal reliability. Various candidates, such as Sn-Ag [14-15], In-Ag [16] or Au-Sn [17-18] alloys fulfill the former requirements. The 80/20 weight percent (w.t.%) Au-Sn alloy has been selected among them. Its physical and thermal properties are described in Table I.

TABLE I. Au-20Sn physical and thermal properties

Young's Modulus (GPa)	59.2
Poisson Ratio	0.3
Yield Strength (MPa)	275
Thermal expansion coefficient (ppm/^{o}C)	15.9
Thermal conductivity (W/mK)	57.3
Specific Heat (J/kg^{o}C)	129
Mass density (kg/m^3)	19720
Melting temperature (^{o}C)	280

As a hard solder it remains in elastic deformation and the thermal expansion coefficient (TEC) mismatch becomes important only when bonding large chips [17-18]. Moreover, its high thermal conductivity provides adequate power dissipation. It is compatible with III-V device metallization and its advantage over other hard solders is the comparatively low melting temperature (280°C), as verified by the binary phase diagram of the Au-Sn alloy [19].

In order to control accurately the alloy composition and accomplish adequate intermixing during fusion, a multilayer structure of the alloy is adopted. In addition to that, rare-earth participation in the solder is exploited by the incorporation of Gd, since rare-earth elements improve adhesion to passivating surfaces, such as SiO_2 [20]. The latter is required, since in the integration process described in [13], III-V dies containing sources and detectors are hosted on an SOI substrate with embedded waveguides to create the complete optical link. The following step is to integrate the optical link over CMOS circuitry lying in wafers with a passivated surface. Therefore, sample bonding via metallization on bare Si as well as on SiO_2 is investigated. Consequently, an initial thin film of 50nm vacuum-evaporated Gd, which corresponds to 3.5w.t.% of the solder, can precede alternating Sn and Au layers of appropriately selected thickness preserving the Au-20Sn eutectic alloy composition. The Sn, Au layers, also deposited by evaporation in vacuum to reduce oxidation, have ranged between 250nm and 750nm in total thickness. Au has been used as a cap layer to prevent alloy surface oxidation. Either full SOI-wafer to CMOS-wafer bonding or SOI-die to CMOS-wafer bonding can be followed.

II. Pattern uniformity and spreading tests

Alloy patterning capability by standard lithography processes has been verified by fabricating pads of varying thickness and diameter on 4-inch Si wafers. Three metallization schemes, according to final pad thickness, have been followed: (i) an 8-layer (Au-20Sn) stack reaching a 250nm thickness, (ii) an 8-layer (Au-20Sn) stack consisting of three times thicker Au, Sn layers reaching a thickness of 750nm, with an initial 50nm Gd layer added, resulting into 800nm total thickness, (iii) the metallization scheme described in (ii) on top of 200nm of either Al or Ti/Cu layers, resulting into 1μm total pad thickness. Scheme (iii), which is more demanding due to larger pattern thickness, has been applied in order to examine solder uniformity above standard CMOS metallization. The ability of precise patterning over both planar and structured substrates has been examined. An example of the latter is shown in a Scanning Electron Microscopy (SEM) photograph (Fig. 1) for an array of pads 1μm thick and 70μm in diameter, fabricated inside etched Si vias 120μm in diameter and 4μm deep. Another SEM photograph (Fig. 2) verifies the 1μm thickness of a pad lying at the center (a), as well as at the wafer edge (b), revealing uniformity across the full 4-inch wafer radius.

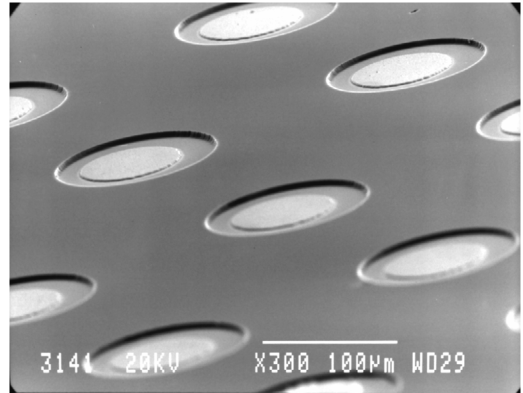
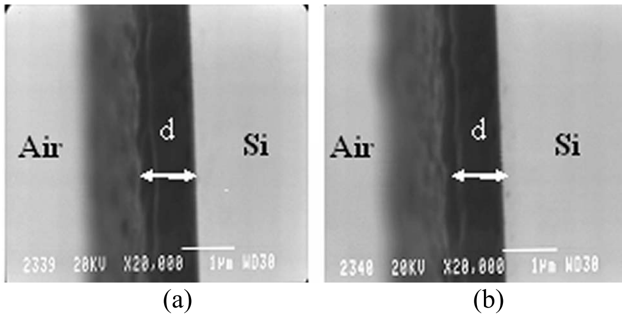


Figure 1. SEM photograph of an array of pads 1μm thick and 70μm in diameter, fabricated inside Si vias 120μm in diameter

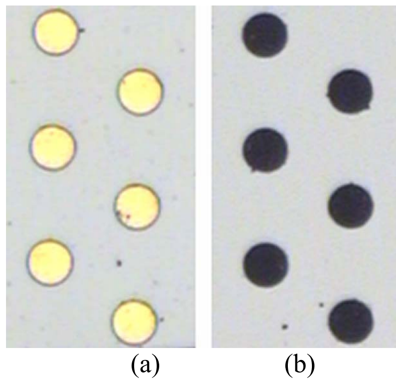
Since contact pads provide point-to-point electrical connectivity to optoelectronic/CMOS devices, their pitch is critical in case of alloy spreading during fusion, which could cause short circuits and therefore device malfunction. To confirm the degree of spreading, samples containing pad arrays were flipped over SiO_2 substrate, while they were annealed at 330°C and pressed by 2.5MPa. In Fig. 3(a), the pad profile before annealing is shown, while in Fig. 3(b) the profile of the same pad is shown. An alloy spreading less than

1μm has been observed. This fact enables dense CMOS/optoelectronic device integration.



(a) (b)

Figure 2. SEM photographs of a 1μm thick pad lying (a) at the center and (b) at the edge of a 4-inch wafer; d stands for pad thickness



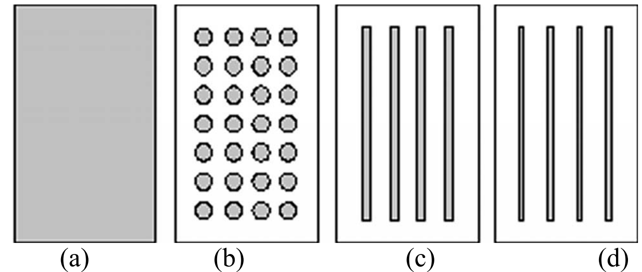
(a) (b)

Figure 3. Light dots on the left (a) stand for the alloy pads before annealing, while dark dots on the right (b) stand for the alloy pads after annealing and pressure were applied.

III. Bonding experiments and quality tests

A variety of bonding experiments have been conducted in order to determine the conditions to be followed for successful bonding results. All bonding experiments took place at an annealing temperature of 330°C in ambient forming gas (95%Arg-5%H_2) for 40min. The eutectic Au-20Sn alloy has as its constituents two intermetallic compounds, namely the ζ (Au_5Sn) and δ (AuSn) phases, due to which the physical and thermal properties of Table I are preserved [17,26]. Although precise control of the 80/20 w.t% is attained, interdiffusion between Sn and Au thin films takes place even at room temperature [17]. This leads to the formation of additional intermetallic compounds, namely the η ($AuSn_4$) and ε ($AuSn_2$) phases, which alter the alloy properties. Since their melting points are 252°C and 309°C respectively, annealing at 330°C eliminates this possibility. When Sn melts (melting temperature 232°C), it wets the adjacent Au layers forming Au-Sn alloys, and liquid as well as solid components interdiffuse. If the temperature is kept above 309°C, the melting point of the solid solution of phases δ and ε, solid-liquid interdiffusion will continue to occur until a uniform layer is obtained. Moreover, the annealing temperature of 330°C is within the allowed post-processing thermal range for CMOS device functionality [21-22]. On the other hand, Sn is expected to segregate to the surface of the Au-rich alloy, due to its lower surface free energy compared to that of Au [17]. This creates a Sn-rich surface layer, which is oxidized even in a very small amount of O_2, i.e. in ambient 95%Arg-5%H_2 gas, despite the retarding influence of H_2 in oxidation. The surface oxide formation, which is a major obstacle for the bonding process, is broken up with pressure application during annealing.

The samples used in bonding experiments have a surface ranging from $0.25cm^2$ to $1.5cm^2$. The topology of the alloy on them is shown in Fig. 4. The pad diameter in Fig. 4(b) is 75μm, the horizontal pitch is 115μm and the vertical pitch is 65μm. The line length in Figs. 4(c) and 4(d) follows sample size from 2.5mm to 15mm respectively, while the line spacing is 2mm. Samples have been fabricated by direct deposition of the Gd-(Au-20Sn) alloy on substrates such as Si, SiO_2 and BCB on Si. Additional samples were fabricated by depositing the Gd-(Au-20Sn) alloy on Al or Ti/Cu layers over Si and SiO_2 substrates to examine the possibility of bonding above standard CMOS metallization schemes. Table II designates the various substrates on which the alloy has been deposited, according to its topology, as described in Fig. 4.



(a) (b) (c) (d)

Figure 4. Topology of dies used in bonding experiments: (a) blanket, (b) pad array, (c) 4 lines of 100μm width and (d) 4 lines of 50μm width

TABLE II. Hosting sample substrates

SAMPLE	(a), (b)	(c), (d)
SUBSTRATE	Si/Si-Al/Si-Ti-Cu	Si, SiO_2
	SiO_2/SiO_2-Ti-Cu	
	BCB	

Table III summarizes the parameters for five experiments using pairs of dies with different

topologies. The total alloy thickness is 800nm, consisting of 50nm Gd followed by 750nm of Sn/Au alternating layers. In the cases (c)-(c) and (d)-(d) 16 cross-section squares are formed with an area of either $(100x100)\mu m^2$ or $(50x50)\mu m^2$, respectively. In Table III, S_{total} stands for the total die area, S_{bond} refers to the contact area between flipped samples and R is the overlap ratio of S_{bond} over S_{total}. P is the pressure applied on the bonding surface (actually flipped dies accept the same force in all cases, while the pressure increases due to decrease of the contacting area) and V_{bond} stands for the total alloy volume participating in bonding. Die shear strength tests for $25mm^2$ samples have shown a $25g/mm^2$ shear stress to be sufficient for detaching the die off the host substrate, revealing edge effects prohibiting the achievement of adequate bonding strength. However, for $150mm^2$ samples, shear strength has exceeded 2.5kg, complying with MIL-STD-883G, Method 2019.7 [23], even if bonding area and overlap ratio are $2mm^2$ (distributed over the substrate, case (a)-(b)) and 1.1% respectively. Table IV summarizes the parameters and results for the cases (a)-(a) and (a)-(b) when the alloy thickness is 250nm, consisting only of Sn/Au alternating layers; Gd has not participated in the alloy in this group of experiments. Row notation is the same as in Table III. Shear tests for this group of samples reveal a very low shear force, which leads to the conclusion that a 250nm thick alloy is incapable of providing adequate bonding strength.

TABLE III. Parameters of bonding experiments with the 800nm thick Gd-(Au-20Sn) alloy

DIE PAIR	(a)-(a)		(a)-(c)	(a)-(b)		(c)-(c)	(d)-(d)
S_{total} (mm^2)	25	150	150	25	150	150	150
S_{bond} (mm^2)	25	150	4	1.1	2	0.16	0.04
R (%)	100	100	2.67	4.4	1.3	0.11	0.03
P (MPa)	0.2	0.03	1.2	4.5	2.5	30.6	122
V_{bond} ($10^{-3}mm^3$)	50	240	6.4	2.2	3.2	0.26	0.06

Moreover, since the proposed methodology is oriented to wafer scale integration, bonding experiments of multiple dies over specific regions of an entire 4-inch wafer have also taken place (Fig. 5). In this case, coarse alignment using alignment marks on the wafer surface and accurate die dicing has been successfully accomplished. For the fine alignment of dies to wafer pads with 10µm accuracy, either a passive or an active alignment methodology should be used [24]. An alignment technique using convex and concave features on both surfaces is under development; however, the former is out of scope of this paper.

TABLE IV. Parameters of bonding experiments with the 250nm thick Au-20Sn alloy

DIE PAIR	(a)-(a)	(a)-(b)
SUBSTRATE	Si	Si
S_{total} (mm^2)	150	
S_{bond} (mm^2)	150	2
R (%)	100	1.33
P (MPa)	0.03	2.47
V_{bond} ($10^{-3}mm^3$)	240	3.2

Figure 5. Four-inch Si wafer with multiple dies bonded on specific regions

IV. Electrical characterization

The metallic bonding technique possesses the advantage of achieving adhesion and electrical connectivity in a single step. The electrical properties of the Au-20Sn alloy are derived through a series of electrical measurements before and after it is annealed. Electrical tests are performed on mm-long alloy lines, which vary from 50µm to 100µm in width. Carrier confinement across such lines ensures consistent results out of I-V testing.

The eutectic Au-20Sn alloy quality before annealing has been verified by resistivity calculations. As an example, the resistance of an alloy line 50µm wide, 11.5mm long and 800nm thick has been measured 34.5Ohm. Inserting the

former data into the resistivity formula, the value of ρ=12·10^{-6}Ohm·cm results for the alloy resistivity. The cited value for the resistivity of the Au-20Sn alloy is 16·10^{-6}Ohm·cm [26]. The slight difference is due to the Gd participation in the alloy.

Typical I-V characteristics for a 4mm long and 50μm wide line before annealing as well as for a 4mm long and 100μm wide line after annealing at 330°C are shown in Fig. 6.

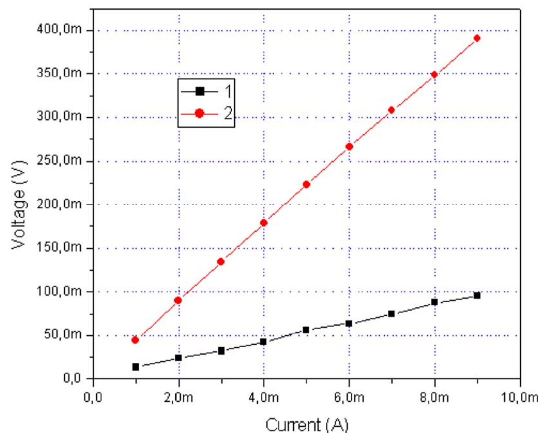


Figure 6. I-V curves for alloy lines 4mm long and (1) 50 μm wide before annealing, (2) 100μm wide after annealing

The I-V curves of Fig. 6 translate into a sheet resistance of 150mOhm/sq and 1.1Ohm/sq before and after the annealing respectively. It has been also observed that the alloy line resistance remains constant for currents as high as 50mA. The resistance increase is due to the different structure of the intermetallic compounds that remain after the annealing, namely the Au_5Sn and AuSn ones [17,19,25]. Their crystal structure is hexagonal (Pearson symbol hP4), while Au and Sn participate in the alloy before annealing in the cubic structure (Pearson symbols cF4 and cF8 respectively). Since the hexagonal solid-state structure is denser than the cubic one, the mean electron-to-ion collision probability is higher, which results into a higher resistance value.

I-V measurements of bonded dies containing similar alloy lines reveal a sheet contact resistance in the range of 500-600mOhm/sq. Since circular pads are used in CMOS to optoelectronic device bonding, the contact resistance as a function of the pad diameter in the range from 10μm to 100μm is plotted in Fig. 7.

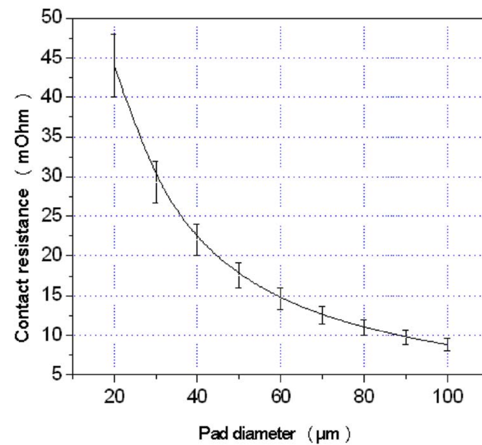


Figure 7. Contact pad resistance versus pad diameter.

Conclusions

A metallic bonding technique permitting dense integration of photonic structures on CMOS wafers has been proposed. A multilayer metallization structure with well-controlled alloy composition has been developed and precise as well as uniform lithographic patterns of the bonding alloy have been reproduced at a 4-inch scale. The ability to achieve bonding of various passivating surfaces and standard interconnect metallizations has been shown. Critical values of the bonding area have been estimated and proof of electrical connectivity of bonded samples has been verified. Electrical measurements have revealed adequate matching between measured and theoretical alloy resistivity and contact sheet resistance in the range of mOhm/sq.

Acknowledgments

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