Optical interconnect for on-chip data communication

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Abstract

It is believed that the concept of integrated optical interconnect is a potential technological solution to alleviate some of the ever more pressing issues involved in exchanging data between cores in SoC architectures (inter-line crosstalk, latency, global throughput, connectivity and power consumption). This abstract summarises work carried out in the framework of the EU-funded PICMOS project on the quantitative comparison of optical interconnect to electrical interconnect in the context of on-chip data communication.

The investigation strategy (evaluation approach, performance metrics) to quantitatively analyse the impact of specifications on both optical and electrical interconnect performance aims at accurately comparing link performance. To enable complete link simulation with transistor-level interface circuits, Verilog-A behavioural models were developed for optical sources, detectors and waveguides. To automatically design both interconnect types following this simulation-based approach, two optimisation toolsets were used (RuneII toolset by LEOM for optical links and ELSA toolset by IMEC/PARIS for electrical links).

In the RuneII toolset, analog design automation techniques were exploited to develop hierarchical synthesis methods for the links and for transistor-level transimpedance amplifier and current-mode source driver interface circuits. The synthesis method is capable of operating over the technology nodes of interest and with varying link-level specification sets, summarised in Table 1. The optimisation strategy that has been chosen minimises the power consumption for a given data rate.

Specification	Value
CMOS technology	{65; 45; 32} nm
BER	1.00E-18 s^{-1}
ITRS max frequency	{2.98; 5.2; 11} GHz
Length	{2500um,20000um}
Activity rate	1
Ambient temperature	70 ℃
V_{dd} (CMOS)	{1.2; 1.1; 1.0} V

Table 1 Specifications for optical link synthesis

The performance metrics taken into account were *static and dynamic power*, *link delay* (measured from electrical input to electrical output), *CMOS area* and *communication density* for optical and electrical links with equal pitch and equal single-link data rate. Electrical links were evaluated in a parallel-wire configuration, including capacitive coupling and crosstalk effects in the power and delay evaluations. The comparison was performed for a number of technologies: predictive technology models for several technology generations (gate lengths down to 32nm) and commercial technologies from STMicroelectronics. For each technology, link simulations were performed for link lengths from 2.5mm up to 2 cm. Figure 1 shows some typical results (here concerning total power comparison).

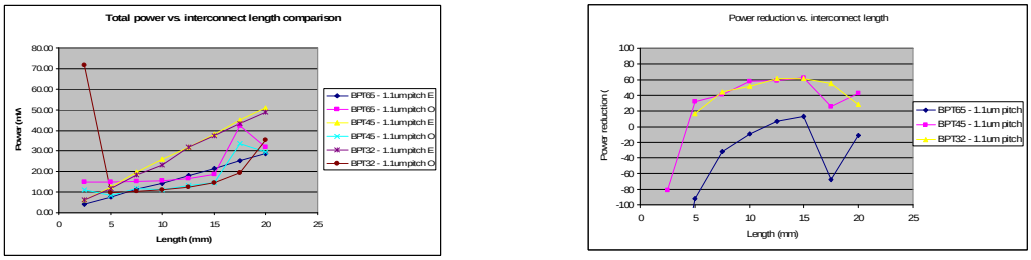

Figure 1 Total power vs interconnect length comparison for 65-45-32nm gate length technologies